

Designing Programmable Logic Array Using Single Spin Logic for Next Generation Nano Scale Device

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ABSTRACT: Spintronics or Spin based electronics is a new emerging technology which has revolutionized in device research in the end of CMOS-topology. The resurgence of Spintronics in post CMOS era has provoked the researchers to explore and to implement the concept of Single Spin Logic (SSL) in digital circuits. In SSL circuits the information is encoded in binary bits '1 & 0' in parallel and anti-parallel spin polarization of single electron confined in quantum dot placed in magnetic field. SSL circuits tantalize the researchers owing to its attributes of high operating speed, high device integrity, low power dissipation that are inevitable for modern electronic circuits. In this article authors attempted to design Programmable Logic Circuits (PLA) using SSL logic circuits in order to design high speed, low power consumption, nonvolatile, exquisite components for next generation nano scale devices.

KEYWORDS: Spintronics, Single Spin Logic, Programmable Logic Array, Quantum Dot

I. INTRODUCTION

In conventional electronic devices the information are stored, processed, and transmitted by the movement of electrons and their charge. In charged based electronic devices, the motion of charges and associated current flow result an unavoidable power dissipation which is the major hindrance to the modern electronic devices. This has prompted the researchers to unearth the alternate ways in order to encode the information. In late 90's a revolutionary idea of researchers has prompted the resurgence of new emerging field called Spintronics or Spin-based electronics. Spintronics is generic name for spin based electronic devices that rendered the researchers to explore SSL circuits in order to design various CMOS based Boolean circuits [1-4]. Apart from combinational and sequential circuits researchers also designed various complex circuits using SSL such as ALU, Glitch Elimination Circuit etc. [5-6]. The intrinsic spin of electron can be of two spin states which is denoted as 'Up Spin' and 'Down Spin' which are marked as Up and Down arrow respectively. In SSL the information is encoded in classical binary bit '1' and '0' in orthogonal spin polarization of single electron confined in a quantum dot placed in magnetic field [7-10]. In lieu of storing the charges in SSL the logical signal is communicated with neighboring devices through the interaction between neighboring spins without any wire.

This article narrates the designing of Programmable Logic array (PLA) using SSL in order to design for next generation nano scale device. This article also evokes a comparative study between conventional PLA and SSL oriented PLA with respect to cost, processing speed, power consumption, power dissipation, and device integrity.

II. WORKING PRINCIPLE

The operation of spintronic devices depend on opposite spin orientation between two electron cells and these neighboring electrons can interact with each other. Here one of the neighboring electron has upward orientation (logic 1) and other one has downward orientation and the resultant electron confined in a quantum dot is either upward (as logic 1) and the downward (as logic 0). In this manuscript authors consider A, B, C as logic input denoted as up spin as logic 1 = \uparrow and the corresponding NOT gates are also designed as down spin as logic 0 = \downarrow . From each of these a NAND gate is designed and later AND gate is produced. Later all the inputs are fed into the AND gates and output of AND gates are complemented by using De Morgan's Theorem and finally they are fed to OR gates. The output of OR is then fed to XOR gates which are connected to logic 1 and logic 0. Using logic 1 and logic 0 we get the desired output of the XOR gate as F_1 and F_2 respectively. The SSL based Programmable Logic Array is illustrated in Fig.1. The red dot represents buffer.

The Boolean Function of PLA is given as
 $F_1 = A\downarrow B\uparrow + A\uparrow C\downarrow + A\downarrow B\uparrow C\downarrow$
 $F_2 = A\uparrow C\downarrow + B\downarrow C\uparrow$

III. COMPARATIVE STUDY

Following is a comparative study based on the attributes of CMOS and SSL based PLA configurations and it includes the cost effective analysis also.

Features	Conventional PLA	Single Spin Logic Oriented PLA
Cost	Higher	Would be much less
Power Consumption	3.5v	<1mV
Power Dissipation	More	Less
Speed & Device Integrity	Low	High and 12000 times faster

IV. LIST OF FIGURES

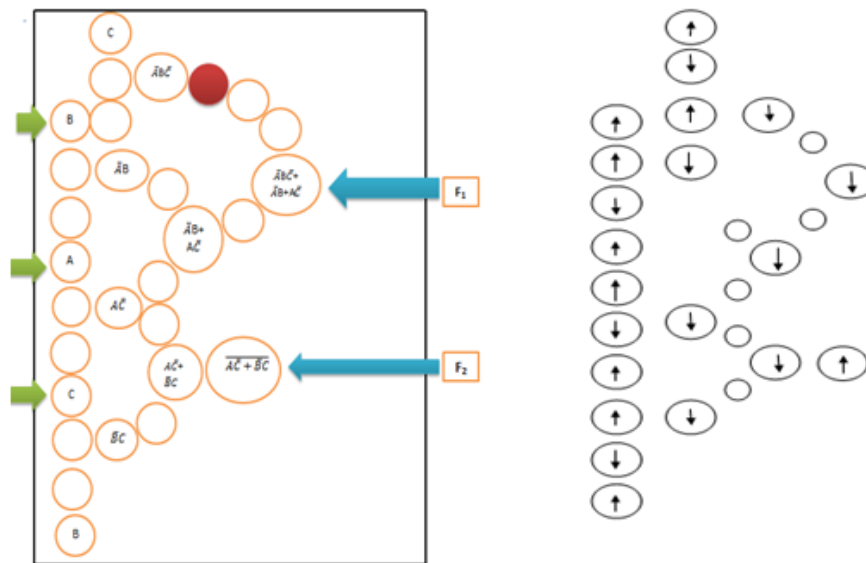


Fig1.SSLOriented Programmable Logic Array and one of its Spin sequence

V. CONCLUSION

To increase the efficiency of IC, SSL has been studied analytically in this manuscript. Consequently the power consumption of the circuit drastically goes down when compared to conventional PLA. Moreover speed mobility and power dissipation shows enhanced acceptability. Thus such design is expected to mobilize the next generation nano scale device.

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